Please amend claims 2-3. 7-9, 11, 13-14, and 16-18 as follows:

1. canceled

2. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim ~~1~~ 7 wherein each of said plurality of FETs having said device structure extending in said single direction include each of said plurality of FETs having a width extending in a first direction and length extending in a second direction; said first and second directions being offset by 90°.

3. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim ~~1~~ 7 wherein said plurality of FETs include a plurality of both N-channel field effect transistors (NFETs) and P-channel field effect transistors (PFETs).

4. (original) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim 3 wherein said storage cell includes a pair of inverters, each inverter formed by one PFET and one NFET connected between voltage supply rail and ground connections and having a common gate connection of said one PFET and one NFET connected to an output of said other one of said pair of inverters.

5. (original) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim 4 wherein said voltage supply rail and ground connections includes said first metal layer.

6. (original) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim 4 wherein said common gate connection of said one PFET and one NFET includes said polysilicon layer.

7. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation ~~as recited in claim 1 wherein~~ comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal local interconnect disposed on said diffusion and polysilicon layers for electrically connecting said diffusion and polysilicon layers and a metal contact extending between said metal local interconnect and said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a wordline; said wordline including a single wordline for implementing one-port operation or two separate wordline connections for implementing two-port operation.

8. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim 1 wherein

comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal contact disposed on said diffusion and polysilicon layers and extending to said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a wordline; said wordline including a single wordline for implementing one-port operation or two separate wordline connections for implementing two-port operation.

9. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port or two-port operation as recited in claim 1 wherein comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a conduction layer disposed on a butted diffusion connection of diffusion-p type and diffusion-n type and a metal local interconnect disposed on said conduction layer; and

each of said pair of wordline FETs having a gate input connected to a wordline; said wordline including a single wordline for implementing one-port operation or two separate wordline connections for implementing two-port operation.

10. canceled

11. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port operation as recited in claim ~~10~~ 13 wherein each of said plurality of FETs having said device structure extending in said single direction include a plurality of both N-channel field effect transistors (NFETs) and P-channel field effect transistors (PFETs) and each of said plurality of NFETs and PFETs having a width extending in a first direction and length extending in a second direction; said first and second directions being offset by 90°.

12. (original) A compact static random access memory (SRAM) cell layout for implementing one-port operation as recited in claim 11 wherein said storage cell includes a pair of inverters, each inverter formed by one PFET and one NFET connected between voltage supply rail and ground connections and having a common gate connection of said one PFET and one NFET connected to an output of said other one of said pair of inverters.

13. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port operation ~~as recited in claim 10 wherein~~ comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal local interconnect disposed on said diffusion and polysilicon layers for electrically connecting said diffusion and polysilicon layers and a metal contact extending between said metal local interconnect and said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a single wordline for implementing one-port operation.

14. (currently amended) A compact static random access memory (SRAM) cell layout for implementing one-port operation ~~as recited in claim 10 wherein~~ comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal contact disposed on said diffusion and polysilicon layers and extending to said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a single wordline for implementing one-port operation.

15. canceled

16. (currently amended) A compact static random access memory (SRAM) cell layout for implementing two-port operation ~~as recited in claim 15 wherein~~ comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal local interconnect disposed on said diffusion and polysilicon layers for electrically connecting said diffusion and polysilicon layers and a metal contact extending between said metal local interconnect and said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a respective wordline of two separate wordline connections for implementing two-port operation.

17. (currently amended) A compact static random access memory (SRAM) cell layout for implementing two-port operation ~~as recited in claim 15 wherein~~ comprising:

a plurality of field effect transistors (FETs); said plurality of FETs defining a storage cell and a pair of wordline FETs coupled to said storage cell; each of said plurality of FETs having a device structure extending in a single direction;

said device structure of each of said plurality of FETs including a diffusion layer, a polysilicon layer and first metal layer;

a local interconnect connecting said diffusion layer, said polysilicon layer and said first metal layer; said local interconnect ~~includes~~ including a metal contact disposed on said diffusion and polysilicon layers and extending to said first level metal for electrically connecting said diffusion and polysilicon layers and said first level metal; and

each of said pair of wordline FETs having a gate input connected to a respective wordline of two separate wordline connections for implementing two-port operation.

18. (currently amended) A compact static random access memory (SRAM) cell layout for implementing two-port operation as recited in claim ~~15~~ 16 wherein each of said plurality of FETs having said device structure extending in said single direction include a plurality of both N-channel field effect transistors (NFETs) and P-channel field effect transistors (PFETs) and each of said plurality of NFETs and PFETs having a

width extending in a first direction and length extending in a second direction; said first and second directions being offset by 90°.

19. (original) A compact static random access memory (SRAM) cell layout for implementing two-port operation as recited in claim 18 wherein said storage cell includes a pair of inverters, each inverter formed by one PFET and one NFET connected between voltage supply rail and ground connections and having a common gate connection of said one PFET and one NFET connected to an output of said other one of said pair of inverters.